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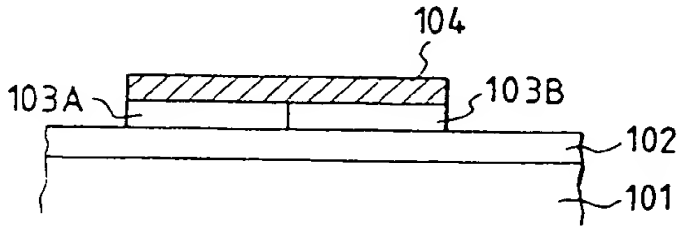
(54) **Semiconductor device and method for producing the same.**

(57) A semiconductor device, wherein an electrode wiring, which is in contact with semiconductor layers of mutually different conductive types and serves to connect at least the layers of mutually different conductive types, comprises a first portion principally composed of a component same as the principal component of the semiconductor layers, and a second portion consisting of a metal.

FIG. 1B



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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor integrated circuit device such as a memory or a signal processing device for use in various electronic appliances, and a method for producing the same.

Related Background Art

Doped polysilicon layer has been used as a wiring material for various semiconductor devices, a gate material for a MOSFET, or an impurity diffusion source. Such doped polysilicon has contained the impurity of a single conductive type, in consideration of ease of manufacturing process.

However, in case polysilicon is used as the gate material of a CMOSFET of the conventional structure, electrodes of a same conductive type, such as n-polysilicon for both NMOSFET and PMOSFET, and the threshold voltages of the two may not be mutually matched.

Also in case of a circuit is composed of NPN and PNP transistors, the polysilicon of a conductive type can only be used, as the emitter diffusion source, in either transistor.

Besides the polysilicon has been associated with drawbacks of giving rise to a large chip size and a loss in the level of integration, because of its high resistance, requiring a large cross-sectional area for reducing the resistance of wiring.

SUMMARY OF THE INVENTION

In consideration of the foregoing, the object of the present invention is to increase the freedom of use of polysilicon of different conductive types, or the freedom in circuit design, and to reduce the chip size thereby improving the level of integration of semiconductor devices.

The semiconductor device of the present invention is featured by a fact that an electrode wiring provided in contact with semiconductor layer of mutually different conductive types and serving at least connecting the areas of said different conductive types comprises a first portion principally composed of a component same as the principal component of said semiconductor layers, and a second portion composed of a metal.

Also the producing method of the present invention is featured by forming a first layer bridging two areas of a semiconductor substrate, exposed in at least two apertures in an insulation film formed on the surface of said semiconductor substrate, said first layer being principally composed of a component same as the principal component of said semiconductor, and depositing A1 or a metal principally composed of A1 selectively on said doped polycrystalline Si layer.

According to the present invention, a metal film is selectively deposited on silicon with different conductive types. It is therefore rendered possible to reduce the wiring resistance, to improve the level of integration, and to improve the freedom in circuit design.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B are schematic views showing the principle of the present invention;
Figs. 2 to 5 are views showing an example of the apparatus adapted for use in the method of the present invention for producing the semiconductor circuit device;
Figs. 6A to 6D are schematic perspective views showing the steps for forming a first wiring layer in the method of the present invention;
Figs. 7 and 8 are respectively a schematic cross-sectional view and a schematic plan view of a CMOSFET constituting an embodiment of the present invention;
Figs. 9 to 12 are schematic cross-sectional views showing the producing method therefor;
Fig. 13 is a circuit diagram of an inverter circuit embodying the present invention;
Figs. 14 to 16 are views showing laminate structures according to the present invention;
Fig. 17 is a plan view of a CMOSFET obtained by a conventional method;
Figs. 18 and 19 are respectively a schematic cross-sectional view and a schematic plan view of a bipolar transistor embodying the present invention;
Figs. 20 to 25 are schematic cross-sectional views showing the producing method therefor;
Fig. 26 is a circuit diagram of a buffer circuit embodying the present invention; and
Fig. 27 is a plan view of a bipolar transistor obtained by a conventional method.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, the present invention will be clarified in detail by preferred embodiments thereof.

Figs. 1A and 1B are respectively a plan view and a cross-sectional view along a line A-A' in Fig. 1A, schematically showing a CMOSFET involving a laminate structure of a polysilicon layer and a metal layer of the present invention. On a semiconductor substrate 101, there are formed a PMOS device (P1) and an NMOS device (N1) are formed to constitute a CMOS circuit. On an oxide film 102, there is formed a laminate electrode wiring consisting of a single polysilicon layer 103 and a metal layer 104, serving as the gate electrodes and wirings for both devices, and source-drain electrodes 106 are further formed. Said single polysilicon layer 103 is doped in p-type in a portion 103A at the side of the PMOS device, and in n-type in a portion 103B at the side of the NNOS device, and, on the entire area of the polysilicon layer, there is deposited selectively a metal layer 104 composed of Al or principally of Al, or of another metal such Cu, Mo or W. A multi-layered wiring may also be obtained by opening a through-hole in an arbitrary position in an insulation film (not shown) formed on the metal wiring layer 104, selectively depositing metal in said through-hole, and forming another wiring on said insulation film.

More specifically, a laminate structure of a metal and a material principally composed of a component same as the principal component (Si in this case) constituting the semiconductor device can be obtained by the above-explained selective deposition, and the multi-layered wiring structure can be obtained by effecting the selective deposition and the non-selective deposition of the conductive materials in succession according to the necessity.

Preferred examples of the metal principally composed of Al include Al-Si, Al-Ti, Al-Cu, Al-Si-Ti and Al-Si-Cu.

The polysilicon layer may have an undoped portion between the p- and n-doped portions. Also a silicide layer may be formed on the polysilicon, prior to selective deposition of metal film.

The doping of the polysilicon layer may be conducted in the ion implantation step for forming the source-drain areas of the MOSFET, or in another separate step. Also the lead electrode for the source-drain area may be composed of a multi-layered film composed of polysilicon and Al-Si.

The laminate structure of polysilicon and metal may be employed in the lead electrode for the emitter and/or collector of a bipolar transistor.

As examples of usable metal, selective deposition of Cu can be achieved with copper bisacetylacetonate, Mo with $Mo(CH_3)_6$, or W with $W(CH_3)_6$ on polysilicon.

In the following there will be explained a deposition method suitable for forming a metal layer for the electrode wiring of the present invention.

[Film forming method]

In the following there will be explained a film forming method of the present invention, suitable for forming an electrode.

Said method is adapted for filling an aperture with a conductive material, for forming the electrode of the above-explained structure.

Said film forming method consists of forming a deposited film by a surface reaction on an electron donating substrate, utilizing alkylaluminum hydride gas and hydrogen gas (said method being hereinafter called Al-CVD method). An aluminum film of satisfactory quality can be deposited by heating the surface of the substrate in the presence of a gaseous mixture particularly consisting of monomethylaluminum hydride (MMAH) or dimethylaluminum hydride (DMAH) as the raw material gas and hydrogen as the reaction gas. At the selective Al deposition, the substrate surface is preferably maintained at a temperature at least equal to the decomposition temperature of alkylaluminum hydride but lower than 450°C, more preferably between 260°C and 440°C, by direct or indirect heating.

The heating of the substrate in the above-mentioned temperature range may be achieved by direct or indirect heating, but formation of an Al film of satisfactory quality can be achieved with a high deposition speed, particularly by direct heating. For example, with the more preferred temperature range of 260° - 440°C, a satisfactory film can be obtained with a deposition speed of 300 - 5000 Å/min. which is higher than in the resistance heating. Such direct heating (substrate being heated by direct transmission of energy from the heating means) can be achieved by heating with a lamp such as a halogen lamp or a xenon lamp. Also indirect heating may be achieved for example by resistance heating, conducted by a heat generating member provided in a substrate support member, for supporting the substrate to be subjected to film deposition, provided in a film depositing space.

This method, if applied to a substrate having both an electron donating surface area and an electron non-donating surface area, allows to form single crystal of aluminum with satisfactory selectivity solely on the electron donating surface area. Such aluminum is excellent in all the properties required for the electrode/wiring material, including a low hillock frequency and a low alloy spike frequency.

This is presumably because the semiconductive or conductive surface constituting an electron donating surface can selectively develop an aluminum film of satisfactory quality and excellent crystalline character of said Al film excludes or significantly reduces the alloy spike formation etc. resulting from an eutectic reaction with the underlying silicon. Such Al film, when employed as an electrode of a semiconductor device, provides the advantages far exceeding the concept of the conventional Al electrode and not anticipated in the prior technology.

As explained above, the Al deposited in an aperture with an electron donating surface, for example an aperture formed in an insulating film and exposing the surface of a semiconductor substrate therein, has a monocrystalline structure. Besides said Al-CVD method can achieve selective deposition of following metal films principally composed of aluminum, with likewise satisfactory quality.

For example, the electrode may be formed by selective deposition of various conductive materials such as Al-Si, Al-Ti, Al-Cu, Al-Si-Ti or Al-Si-Cu by the use of a mixed gaseous atmosphere employing, in addition to alkylaluminum hydride gas and hydrogen, a suitable combination of:

Si-containing gas such as SiH_4, Si_2H_6, Si_3H_8, $Si(CH_3)_4$, $SiCl_4$, SiH_2Cl_2 or $SiHCl_3$;

Ti-containing gas such as $TiCl_4$, $TiBr_4$ or $Ti(CH_3)_4$; and/or

Cu-containing gas such as copper bisacetylacetonate $Cu(C_5H_7O_2)_2$, copper bisdipyvaloylmethanite $Cu(C_{11}H_{19}O_2)_2$ or copper bishexafluoroacetylacetonate $Cu(C_5HF_6O_2)_2$.

Also since said Al-CVD method is excellent in selectivity and provides satisfactory surface characteristics on the deposited film, there can be obtained a metal film suitable and widely usable for the wirings of a semiconductor device, by employing a non-selective film forming method in a next deposition step to form a metal film composed solely or principally of aluminum not only on the selectively deposited aluminum film mentioned above but also on the SiO_2 insulation film.

Examples of such metal films include combinations of selectively deposited Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti or Al-Si-Cu and non-selectively deposited Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti or Al-Si-Cu. Said non-selective film deposition may be achieved by CVD other than the aforementioned Al-CVE, or by sputtering.

[Film forming apparatus]

In the following there will be explained a film forming apparatus suitable for the electrode formation according to the present invention.

Figs. 2 to 4 schematically illustrate a continuous metal film forming apparatus suitable for executing the film forming method explained above.

As shown in Fig. 2, said apparatus is composed of a load lock chamber 311, a CVD reaction chamber (first film forming chamber) 312, an Rf etching chamber 313, a sputtering chamber (second film forming chamber) 314 and a load lock chamber 315, which are rendered sealable from the external atmosphere and mutually communicatable by means of gate valves 310a - 310f and can be respectively made vacuum or reduced in pressure by vacuum systems 316a - 316e. The load lock chamber 311 is used for eliminating the atmosphere of substrate and replacing it with H_2 prior to the deposition, in order to improve the throughout. The next CVD reaction chamber 312, for selective deposition onto the substrate under normal or reduced pressure, is provided therein with a substrate holder 318 with a resistance heater 317 for heating the substrate surface subjected to film formation at least within a temperature range of 200°-450°C, and receives the raw material gas such as of alkylaluminum hydride, which is gasified by bubbling with hydrogen in a bubbler 319-1, through a raw material gas supply line 319, and hydrogen as the reaction gas through a gas line 319'. The Rf etching chamber 313, for cleaning (etching) of the substrate surface in Ar atmosphere after the selective deposition, is provided therein with a substrate holder 320 capable of heating the substrate at least within a range of 100° - 250°C and an Rf etching electrode line 321, and is connected to an Ar gas supply line 322. The sputtering chamber 314, for non-selective deposition of a metal film by sputtering in Ar atmosphere, is provided therein with a substrate holder 323 to be heated at least within a range of 200° - 250°C and a target electrode 324 for mounting a sputtering target 324a, and is connected to an Ar gas supply line 325. The final load lock chamber 315, for adjustment of the substrate after metal film deposition and prior to the exposure to the external atmosphere, is designed to be capable of replacing the atmosphere with N_2.

Fig. 3 shows another example of the continuous metal film forming apparatus, wherein same components as those in Fig. 2 are represented by same numbers. The apparatus in Fig. 3 is different from that in Fig. 2 in that the substrate surface is directly heated by halogen lamps 330, and, for this purpose, the substrate holder 312 is provided with projections 331 for supporting the substrate in a floating state.

Direct heating of the substrate surface with such structure further increases the deposition speed as explained before.

The continuous metal film forming apparatus of the above-explained structure is equivalent, in practice, to a structure shown in Fig. 4, in which the load lock chamber 311, CVD reaction chamber 312, Rf etching chamber 313, sputtering chamber 314 and load lock chamber 315 are mutually combined by a transport chamber 326.

In this structure, the load lock chamber 311 serves also as the chamber 315. In said transport chamber 326, there is provided an arm 327 constituting transport means, rotatable in both directions A-A and extendable and retractable in direction B-B, whereby the substrate can be transferred in succession from the load lock chamber 311 to the CVD reaction chamber 312, Rf etching chamber 313, sputtering chamber 314, and finally to the load lock chamber 315 without exposure to the external atmosphere, as indicated by arrows in Fig. 5.

[Film forming process]

Now there will be explained the film forming process for forming the electrodes and wirings according to the present invention.

Fig. 6 illustrates the film forming procedure for forming the electrodes and wirings according to the present invention, in schematic perspective views.

At first the outline of the procedure will be described. A semiconductor substrate with an insulating film having apertures therein is placed in the film forming chamber, and the surface thereof is maintained for example at 250° - 450°C. Thermal CVD conducted in a mixed atmosphere of DMAH gas as alkylaluminum hydride and hydrogen gas causes selective deposition of Al on the semiconductor exposed in the apertures. There may naturally be conducted selective deposition of a metal film principally composed of Al, for example Al-Si, by introduction for example of Si-containing gas, as explained before. Then a metal film composed solely or principally of Al is non-selectively formed by sputtering, on the selectively deposited Al and on the insulation film. Subsequently the non-selectively deposited metal film is patterned into the shape of desired wirings, thereby obtaining the electrodes and the wirings.

This procedure will be explained in greater details with reference to Figs. 3 and 6. At first prepared is a substrate, consisting for example of a monocrystalline silicon wafer bearing thereon an insulation film, in which apertures of different sizes are formed.

Fig. 6A schematically shows a part of said substrate, wherein shown are a monocrystalline silicon substrate 401 constituting a conductive substrate; a thermal silicon oxide film 402 constituting an insulation film; and apertures 403, 404 of different sizes.

The formation of Al film, constituting a first wiring layer, on the substrate is conducted in the following manner, with the apparatus shown in Fig. 3.

At first the above-explained substrate is placed in the load lock chamber 311, in which a hydrogen atmosphere is established by introduction of hydrogen as explained before. Then the reaction chamber 312 is evacuated by the vacuum system 316b approximately to 1×10^{-8} Torr, though Al film formation is still possible with a higher pressure.

Then DMAH gas obtained by bubbling is supplied from the gas line 319, utilizing H_2 as the carrier gas.

Also hydrogen as the reaction gas is introduced from the second gas line 319', and the interior of the reaction chamber 312 is maintained at a predetermined pressure, by the adjustment of an unrepresented slow leak valve. A typical pressure is about 1.5 Torr. DMAH is introduced into the reaction chamber from the DMAH line, with a total pressure of about 1.5 Torr and a DMAH partial pressure of about 5.0×10^{-3} Torr. Then the halogen lamps 330 are energized to directly heat the wafer, thereby causing selective Al deposition.

After a predetermined deposition time, the DMAH supply is interrupted. Said deposition time is so selected that the Al film on Si (monocrystalline silicon substrate 1) becomes equally thick as SiO_2 (thermal silicon oxide film 2), and can be experimentally determined in advance.

In this process, the substrate surface is heated to ca. 270°C by direct heating, and the procedure explained above causes selective deposition of an Al film 405 in the aperture, as shown in Fig. 6B.

The foregoing is called a first film forming step for forming an electrode in an aperture.

After said first film forming step, the CVD reaction chamber 312 is evacuated, by the vacuum system 316b, to a pressure not exceeding 5×10^{-3} Torr. Simultaneously the Rf etching chamber 313 is evacuated to a pressure not exceeding 5×10^{-6} Torr. After confirmation of said evacuations of the chambers, the gate valve 310c is opened, then the substrate is moved from the CVD reaction chamber 312 to the Rf etching chamber 313 by the transport means, and said gate valve is closed. The Rf etching chamber 313 is evacuated to a pressure not exceeding 10^{-6} Torr, and is then maintained in argon atmosphere of 10^{-1} - 10^{-3} Torr by argon supply from the supply line 322. The substrate holder 320 is maintained at ca. 200°C, and an Rf power of 100 W is supplied to the Rf etching electrode 321 for about 60 seconds to generate an argon discharge in said chamber 313, whereby the substrate surface is etched with argon ions and the unnecessary surfacial layer of the CVD deposition film can be eliminated. The etch depth in this case is about 100 Å, corresponding to the oxide film. Said surface etching of the CVD deposition film, conducted in the RF etching chamber, may be dispensed with since said surfacial layer is free from oxygen etc. as the substrate is transported in vacuum. In such case, the Rf etching chamber 313 may serve for varying the temperature within a short time if the temperature is significantly different between the CVD reaction chamber 312 and the sputtering chamber 314.

After said Rf etching, the argon supply is terminated, and the Rf etching chamber 313 is evacuated to 5 x

source-drain areas 8, n-type gate polysilicon 10, an Al-Si film 11 selectively deposited thereon, and source-drain electrodes 13. The PMOSFET and NMOSFET are electrically separated by a separation area 3. The polysilicon areas 9 and 11 are parts, doped in different conductive types, of a continuous polysilicon layer, and the Al-Si film 11 is selectively deposited on the entire area of said polysilicon layer.

In Fig. 8, 14 indicates contact areas of the source-drain electrodes, and 15 indicates the boundary between the field oxide film 3 and the transistor active area. The source-drain electrode 14 are preferably formed also by the selective deposition method explained above.

Now reference is made to Figs. 9 to 12, for explaining the method for producing the MOSFET shown in Figs. 7 and 8.

At first a predetermined area of an n-type substrate 1 with an impurity concentration of 10^{14} - 10^{16} cm^{-3} was subjected to implantation of B^+ ions with a dose of 10^{12} - 10^{13} cm^{-2}, followed by a heat treatment at 1100 - 1200°C to form a p-area 2. Then a separation area 3 was formed by a LOCOS process, and a gate oxide film 6 of a thickness of 100 - 350 Å was formed (Fig. 9). Subsequently ion implantation was conducted in ordinary manner, in order to control the threshold voltage and the source-drain voltage resistance.

Then a polysilicon layer of a thickness of 1500 - 4500 Å was deposited by LPCVD, then a area where the NMOSFET was to be formed was covered with photoresist 5, and B^+ ions were implanted with a dose of 10^{14} - 3 x 10^{15} cm^{-2} only in the area of PMOSFET (Fig. 10). The photoresist in the NMOSFET area was stripped, the PMOSFET area was newly covered with photoresist, and P^+ ions were implanted with a dose of 5 x 10^{14} - 10^{16} cm^{-2} (Fig. 11). Subsequently heat treatment was conducted at 900 - 1000°C.

After patterning of the polysilicon, the surface and the lateral faces of polysilicon layers 9, 10 were oxidized. Then BF_2^+ ions were implanted with a dose of 10^{15} - 3 x 10^{15} cm^{-2} in order to form the source-drain areas 7 of PMOSFET, and As^+ ions were implanted with a dose of 10^{15} - 10^{16} cm^{-2} in order to form the source-drain areas 8 of NMOSFET. Thus the source-drain areas can be formed in self-aligning manner. Then thermal treatment was conducted at 800-1000°C, and the surfacial oxide film of the polysilicon areas 9, 10 was eliminated by etch back (Fig. 12).

On thus treated semicondudtor substrate, the polysilicon layers 9, 10 and the oxide film exist together as shown in Fig. 12. Among the above-explained Al-CVD method, a low pressure CVD employing DMAH, Si_2H_6 and hydrogen as the reaction gas was conducted to selectively deposite an Al-Si film solely on the polysilicon layers 9, 10, thereby forming a multi-layered film of polysilicon an Al-Si.

Subsequently the CMOSFET shown in Fig. 7 was prepared by depositing the interlayer insulation film 12 by CVD, opening contact holes on the source-drain areas of MOSFET, and depositing Al-Si 13 in said contact holes by selective deposition. A multi-layered wiring structure may be formed by forming a second interlayer insulation film on the structure shown in Fig. 7. This can be achieved by opening through-holes reaching the gate metal electrodes 11 or source-drain electrodes 13 in said second insulation film, filling said through-holes with Al-Si or Al by selective deposition, forming for example an Al-Si film on the second interlayer insulation film by non-selective depositing method such as sputtering, effecting a patterning step in ordinary manner and forming a passivation film.

The CMOSFET thus prepared can be utilized as an inverter as shown in Fig. 13. In Fig. 13, an area below the gate electrode of the PMOSFET is composed of p-polysilicon, while an area below the gate electrode of the NMOSFET is composed of n-polysilicon. When polysilicon is used as the electrode, a pn junction is formed therein so that it has been impossible to utilize polysilicon as a wiring. However the present embodiment has enabled the use of polysilicon as a wiring, for example for a common gate of a CMOS structure, since Al-Si metal is selectively deposited on the polysilicon.

Fig. 14 is a cross-sectional view of a gate wiring Gl of PMOSFET and NMOSFET in Fig. 13. In the present example the p-area 9 and the n-area 10 in polysilicon are in mutual contact, but there may be formed an undoped (i-type) are 16 therebetween as shown in Fig. 15.

As the above-explained selective Al-Si depositing method can selectively deposite Al-Si not only on silicon but also on silicides such as WSi_2, $MoSi_2$, $TiSi_2$ or $TaSi_2$, the wiring may also be formed, as shown in Fig. 16, by forming a silicide 17 on the polysilicon layers, 9, 10 and selectively depositing an Al-Si film 11 thereon.

The ion implantation into polysilicon and the ion implantation for source-drain formation for MOSFET in the present example are conducted in separate steps, but these ion implantations may be in a same step.

It is furthermore possible to use a multi-layered film of polysilicon and Al-Si for the lead electrodes for the source-drain of MOSFET, as in the gate electrodes.

Fig. 17 shows, for the purpose of comparison, a CMOSFET prepared by a conventional process, in a plan view. At the sides of PMOS (PI) and NMOS (NI), there are respectively formed polysilicon gates 109, 110 doped in p-type and n-type, and said gates are connected to an upper Al layer 113 through contacts 114 in through-holes formed in the interlayer insulation film. In such conventional example, a polysilicon wiring with a thickness of 4000 Å, a length of 10 μm and a width of 2 μm had a resistance of 50 - 200 Ω. On the other hand, a wiring

of the present invention with a polysilicon layer of a thickness of 2000 Å and an Al-Si (or Al) layer with a thickness of 4000 Å significantly reduced the resistance to 1 Ω or less. Consequently the switching speed of the CMOS inverter can be significantly increased. Also according to the present invention, since Al-Si is directly deposited on a single polysilicon layer including the portions of different conductive types, the connecting part between Al-Si and polysilicon, as in the conventional structure shown in Fig. 17, can be eliminated. It is therefore possible to eliminate unnecessary areas in the circuit layout. The production yield is not deteriorated by this fact, and the design freedom is increased considerably since n^+-polysilicon and p^+-polysilicon can be freely connected in the circuit. This fact contributes greatly to the improvement of circuit performance and the reduction of period required for circuit development.

Example 2

Fig. 18 is a schematic plan view of an example of bipolar transistor embodying the present invention, and Fig. 19 is a plan view thereof.

This example has an npn transistor N2 and a pnp transistor P2 formed on a semiconductor substrate 31 composed for example of monocrystalline silicon. More detailedly, the substrate 31 is provided with an n^+-buried layer 32 and a p^+-buried layer 33, and the npn transistor (N2) includes an n-type collector lead layer 36 formed in an aperture in an n-epitaxial layer 34, a base layer 38A formed on said n-epitaxial layer 34, an emitter electrode penetrating through an oxide film 37 and composed of polysilicon 40 and an Al-Si film 44 formed thereon, and collector and base Al-Si electrodes 44 connected to the wirings on an interlayer insulation film 43. Under the polysilicon layer 40 there is formed a diffusion layer 40A. Similarly the pnp transistor (P2) includes a collector area 35, a collector contact 38B, a base layer 39, a polysilicon layer 41 constituting an emitter electrode, an Al-Si layer 42 selectively deposited thereon, collector and base Al-Si electrodes 44, and a diffusion layer 41A. The npn transistor N2 and the pnp transistor P2 are electrically separated by a p-type isolation area 35A. In Fig. 19, 43 and 44 are isolation areas for the npn and pnp transistors, and 45 and 46 are contact areas of the emitter electrodes of said transistors.

In the following there will be explained the method for producing the device of the present example, with reference to Figs. 20 to 25.

At first the n-buried layer 32 and the p-buried layer 33 were formed by an ordinary method on a p-silicon substrate 31 with an impurity concentration of 10^{14} - 10^{16} cm^{-3}. Then, as the collector area of the npn transistor, an n-epitaxial layer 34 was deposited with a thickness of 1 - 5 μm and with an impurity concentration of 10^{15} - 10^{16} cm^{-3}, by epitaxial growth (Fig. 20).

Then B^+ ions were implanted with a dose of 10^{12} - 10^{13} cm^{-2} to form the collector area 35 of the pnp transistor and the p-type isolation area 35A. Also P^+ ions were implanted with a dose of 10^{15} - 10^{16} cm^{-2} for forming the n-type collector lead layer 36, for reducing the collector resistance of the pnp transistor. Subsequently a thick oxide film 37 was formed by LOCOS process (Fig. 21).

Subsequently the base area 38A of the npn transistor and the collector contact 38B of the pnp transistor were formed by B^+ ion implantation with a dose of 10^{13} - 10^{14} cm^{-2}, and the base area 39 of the pnp transistor was formed by P^+ ion implantation with a dose of 10^{13} - 10^{14} cm^{-2}. Then, after apertures were formed in the oxide film of the emitter portions of the npn and pnp transistors, the polysilicon layer 51 was deposited. The area of the npn transistor was covered with photoresist 52, and B^+ ions were implanted with a dose of 5×10^{14} - 5×10^{15} cm^{-2} into the area of the pnp transistor (Fig. 22).

Thereafter the photoresist of the npn transistor area was stripped, then the pnp transistor area was covered anew with photoresist 52, and As^+ ions were implanted with a dose of 10^{15} - 10^{16} cm^{-2} into the polysilicon layer of the npn transistor area. Then a heat treatment was conducted at 900 - 1000°C in order to diffuse the impurity of the polysilicon layer into the semiconductor substrate (Fig. 23).

Subsequently the polysilicon layer was patterned to form the emitter electrode polysilicon layer 40 for the npn transistor and the emitter electrode polysilicon layer 41 of the pnp transistor (Fig. 24).

Onto the polysilicon layers 40, 41, Al-Si films 42 were selectively deposited by the aforementioned Al-CVD method, utilizing DMAH gas, Si_2H_6 and H_2 with the substrate surface maintained at 270°C (Fig. 25).

The bipolar transistors shown in Fig. 18 were completed thereafter by depositing the interlayer insulation film 43 by CVD, opening contact holes on the collectors and the bases, and selectively depositing the Al-Si layer 44 similarly as the Al-Si film 42 for the emitter electrode. In the structure shown in Fig. 18, it is possible to form wirings connected to the electrodes 44 by non-selectively depositing an Al-Si film for example by sputtering on the insulation film 43 and effecting a patterning step. Similarly a multi-layered wirings connected to the Al-Si films 42 may be formed.

The bipolar transistors thus formed may be utilized as a buffer circuit as shown in Fig. 26.

In Fig. 26, the emitter of the pnp transistor is composed of p-polysilicon and Al-Si film, while the emitter of

the npn transistor is composed of n-polysilicon and Al-Si film. In the present example, the laminate film composed of polysilicon and Al-Si is utilized in the emitters of the bipolar transistors, but it may also be used in the collector lead electrodes.

Also as explained in the first example, the structure of the polysilicon layer and the Al-Si film at the boundary of the p- and n-areas can be any of the structures shown in Figs. 14, 15 and 16.

Fig. 27 illustrates, for the purpose of comparison, bipolar transistors of a similar structure, prepared by a conventional process. The npn transistor N2 includes an n^+-collector 136, a p-base 138, an n^+-emitter contact 145 and an n^+-polysilicon layer 140. On the other hand, the pnp transistor P2 includes a p^+-collector 138A, an n-base 139, a p^+-emitter contact 146, and a p^+-polysilicon layer 141. The polysilicon layers 140, 141 are connected to an upper Al wiring layer 142, through contacts 147 in through-holes formed in the interlayer insulation film. As will be apparent from comparison of Figs. 19 and 27, the conventional structure involves a longer polysilicon wiring with a higher resistance. On the other hand, according to the present invention, the Al-Si film deposited on polysilicon can reduce the resistance, so that said bipolar transistors can significantly reduce the switching speed when they are utilized in an inverter circuit. Also as explained in the example 1, there can be achieved improvement in the level of integration and increase in the freedom in circuit design.

In the foregoing examples, the Al-Si film is selectively deposited on polysilicon. However it is also possible to convert polysilicon into monocrystalline state by laser annealing or electron beam annealing, and to selectively deposit the Al-Si film on such monocrystalline area. As an Al-Si film of improved crystallinity can be grown on monocrystalline silicon, the migration resistance can be further improved.

In addition to aluminum and metals principally composed of aluminium, it is also possible to selectively deposite a Cu film with copper bisacetylacetonate or copper bisdipyvaloylmethanate and H_2, or a Mo film with $Mo(CH_3)_6$ or $Mo(CO)_6$, or a W film with $W(CH_3)_6$, or an alloy film thereof on silicon, thereby obtaining similar effects as in the foregoing examples.

It is furthermore possible to form bipolar transistors and MOSFET's on a same substrate by combining the first and second examples.

As explained in the foregoing, the present invention allows to reduce the wiring resistance and to achieve satisfactory matching in a complementary circuit, by doping a silicon layer, for example a polysilicon layer, with impurities of different conductive types, and selectively depositing a metal film thereon.

Also it enables to use polysilicon for both contacts and wirings, thereby improving the production yield, reducing the chip size and improving the level of integration.

Also the possibility of connection of n^+-polysilicon and p^+-polysilicon in the circuit significantly increases the freedom of circuit designing, thereby contributing to the improvement in the circuit performance and to the reduction in the period required for device development.

Claims

1. A semiconductor device, wherein an electrode wiring, which is in contact with semiconductor layers of mutually different conductive types and serves to connect at least said layers of mutually different conductive types, comprises a first portion principally composed of a component same as the principal component of said semiconductor layers, and a second portion consisting of a metal.

2. A semiconductor device according to claim 1, wherein said first portion is composed of polycrystalline silicon.

3. A semiconductor device according to claim 1 or 2, wherein said second portion is composed of aluminum or a metal principally composed of aluminum.

4. A semiconductor device according to any of claims 1 to 3, wherein said electrode wiring connects gates of a PMOS transistor and an NMOS transistor of a CMOS circuit.

5. A semiconductor device according to any of claims 1 to 3, wherein said electrode wiring mutually connects emitters or collectors of a pnp transistor and an npn transistor.

6. A method for producing a semiconductor device which comprises forming a first layer composed principally of a component same as the principal component of a semiconductor substrate, said first layer bridging two portions of said semiconductor substrate, exposed in at least two apertures formed in an insulation film provided on the surface of said semiconductor substrate, and selectively depositing aluminum or a

metal principally composed of aluminum on said first layer composed of doped polycrystalline silicon.

7. A method according to claim 6, wherein said deposition of aluminum or a metal principally composed of aluminum effects selective deposition of aluminum by a CVD method utilizing at least alkylaluminum hydride and hydrogen.

8. A method according to claim 6, wherein said deposition of aluminum or a metal principally composed of aluminum effects selective deposition of aluminum containing silicon by a CVD method utilizing at least dimethylaluminum hydride, gas containing silicon atoms and hydrogen.

FIG. 1A

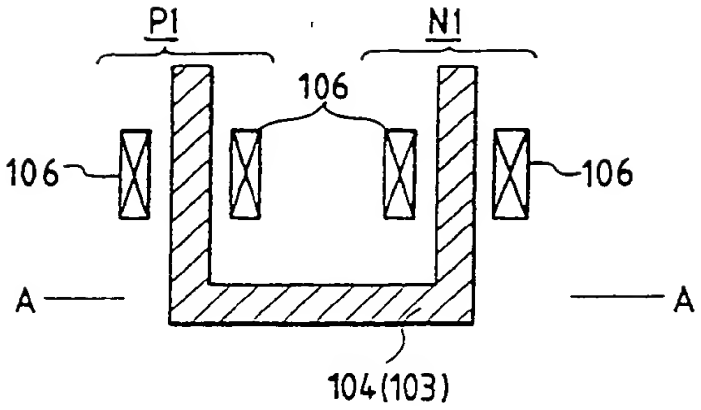


FIG. 1B

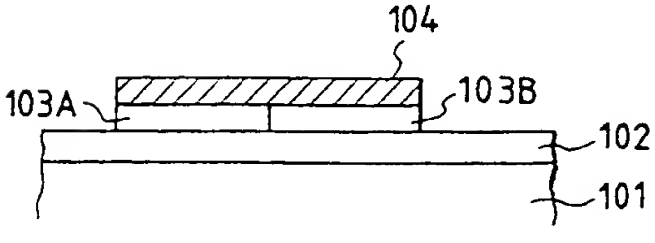
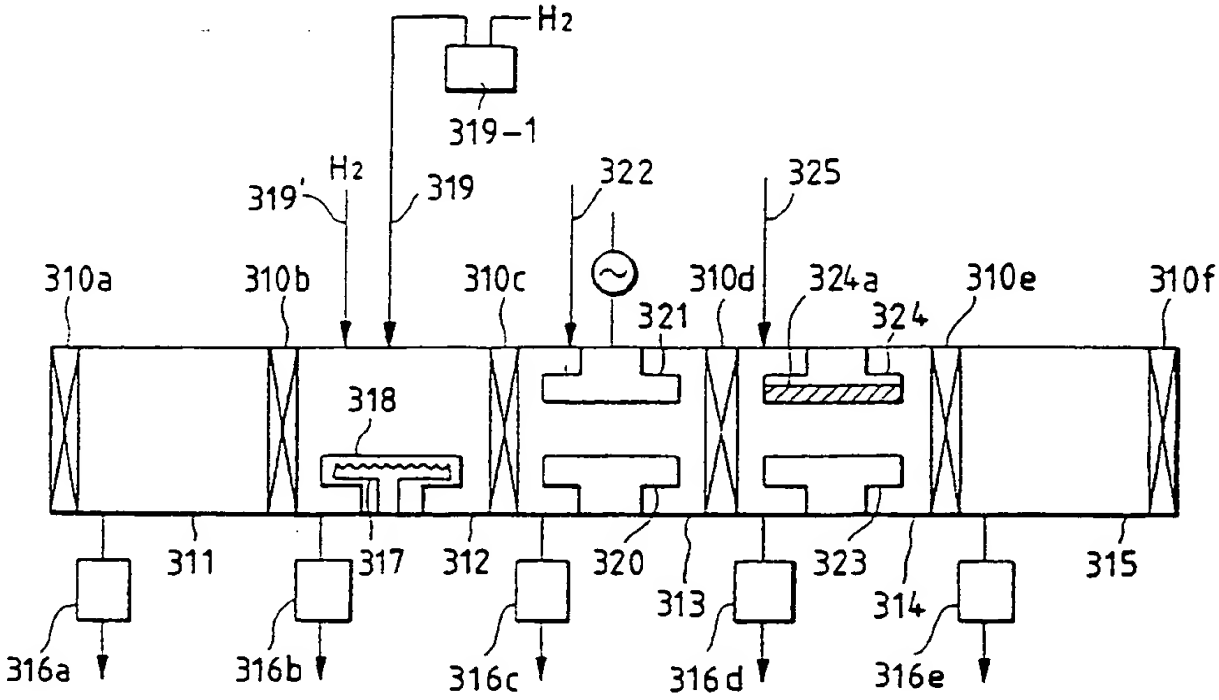


FIG. 2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319-1
319'
H2
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322
325
310a
310b
310c
310d
324a
310e
310f
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324
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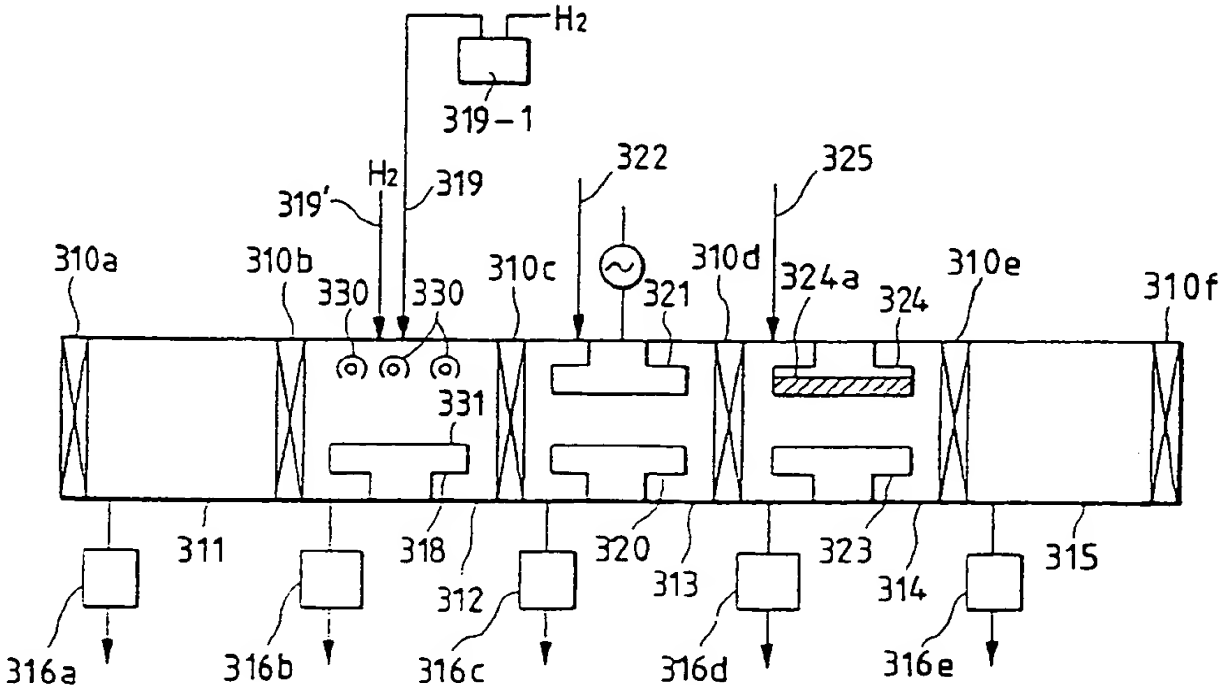
311
317
312
320
313
323
314
315
316a
316b
316c
316d
316e

FIG. 3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319-1
319'
H2
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310b
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310d
324a
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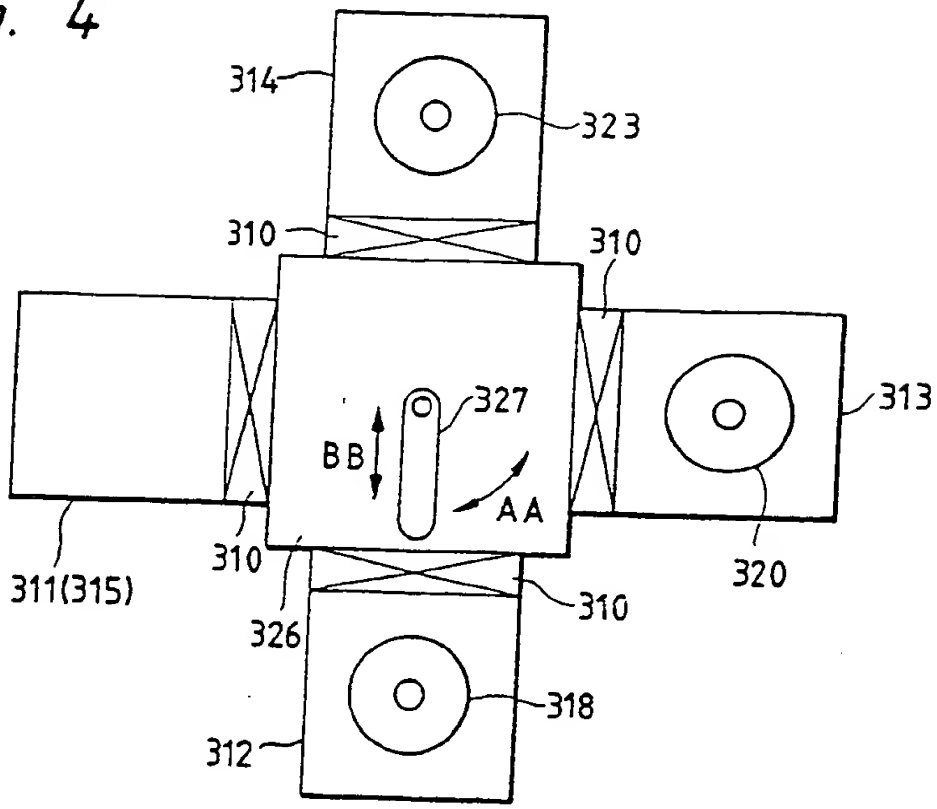
315
316a
316b
316c
316d
316e

FIG. 4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327
BB
AA
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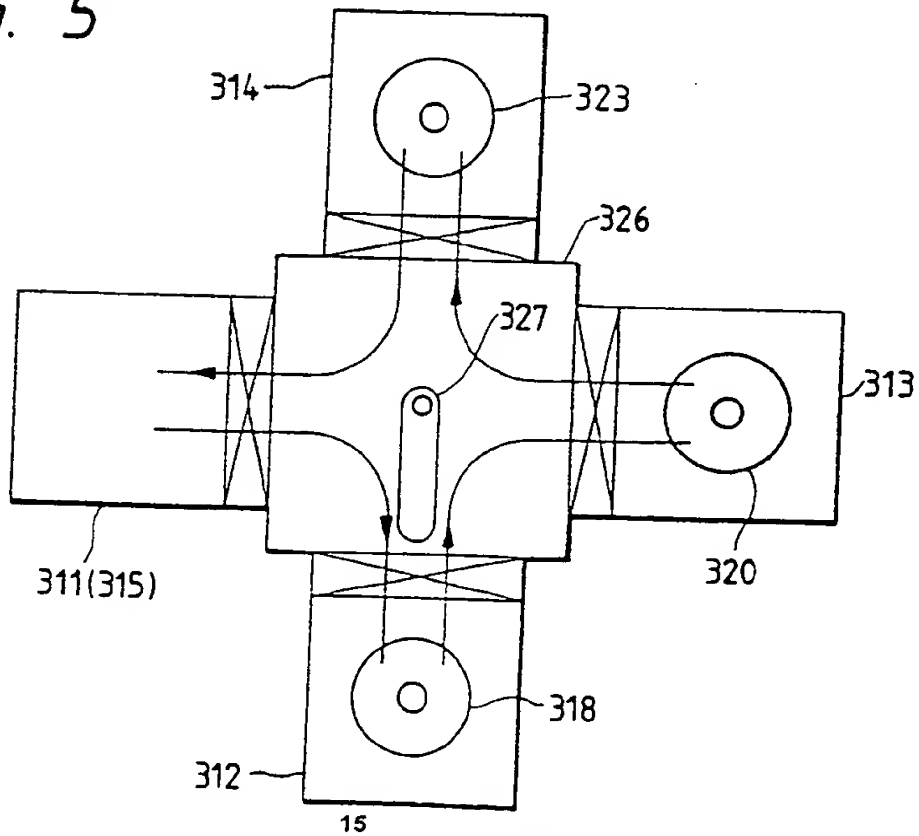
311(315)
320
326
310
318
312

FIG. 5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323
326
327
313
311(315)
320
318
312

FIG. 6A

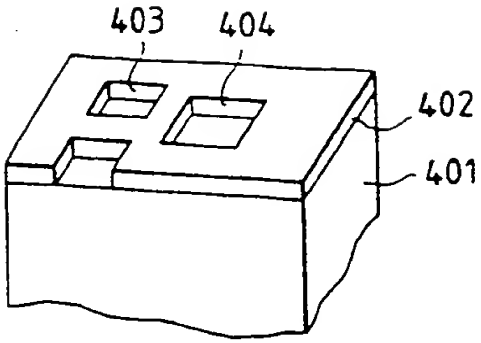


FIG. 6B

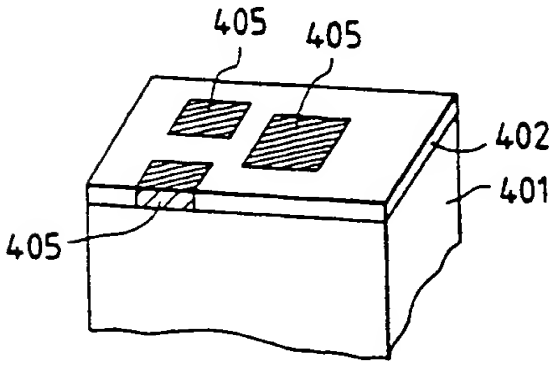


FIG. 6C

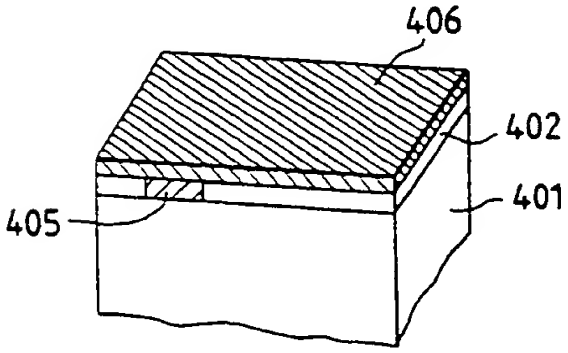


FIG. 6D

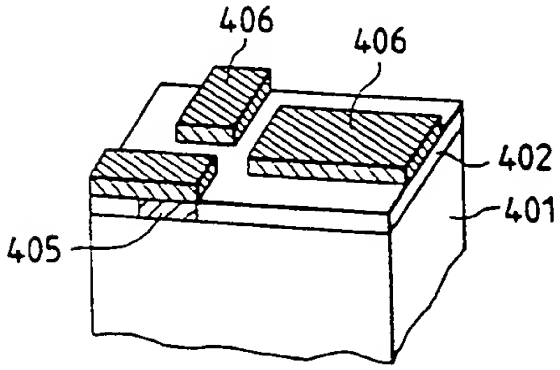


FIG. 7

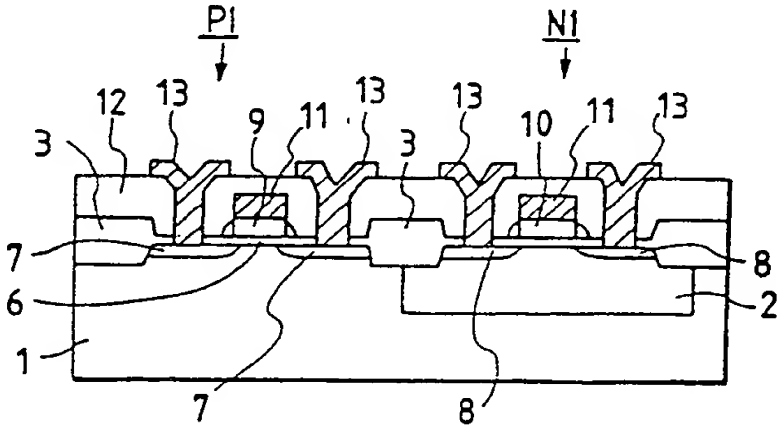


FIG. 8

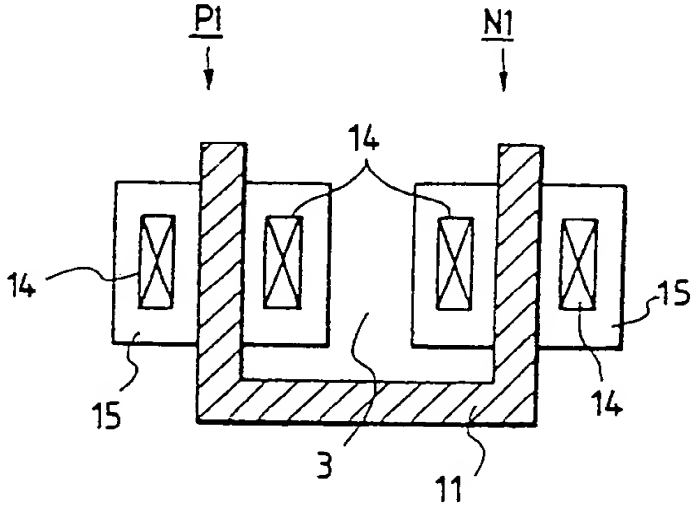


FIG. 9

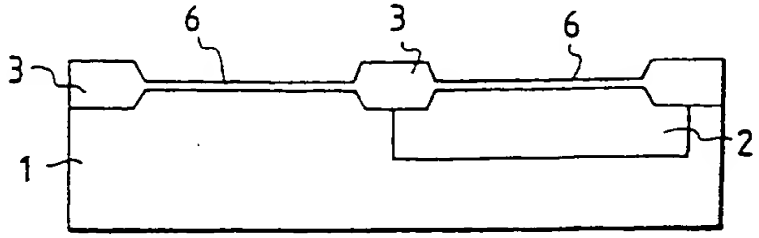


FIG. 10

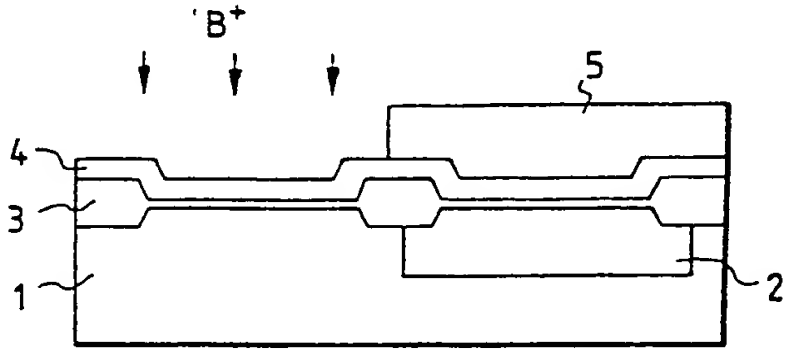


FIG. 11

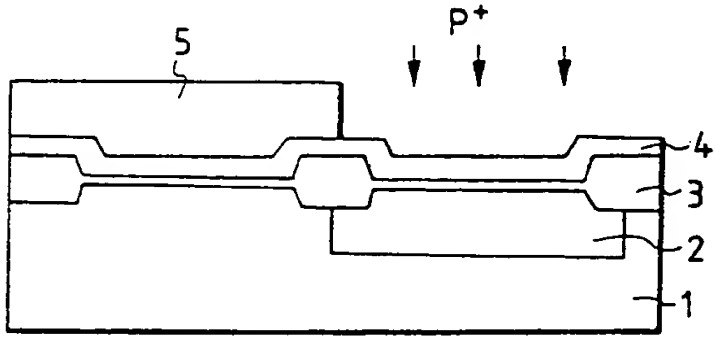


FIG. 12

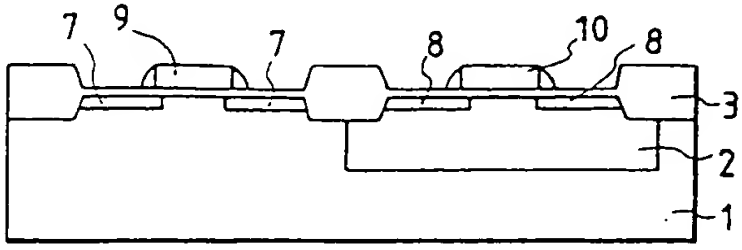


FIG. 13

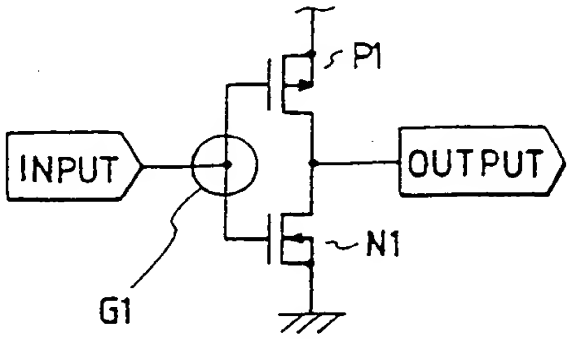


FIG. 15

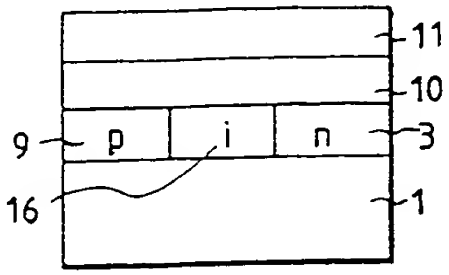


FIG. 14

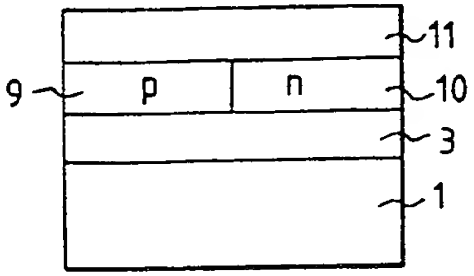


FIG. 16

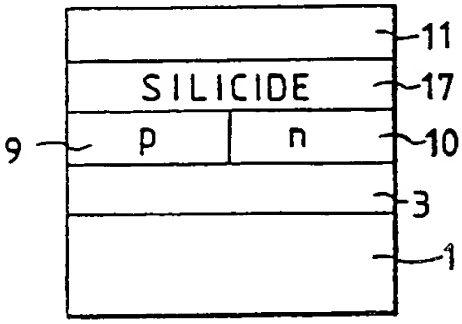


FIG. 17

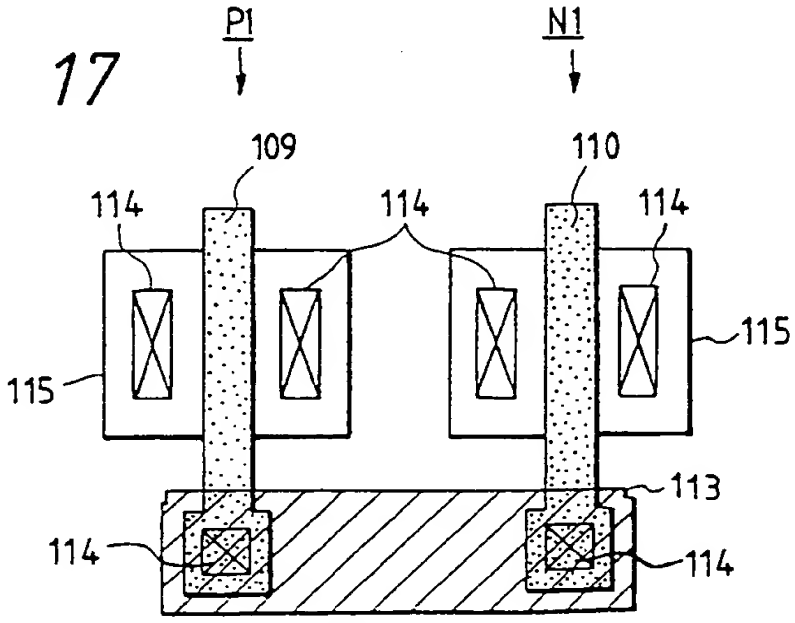
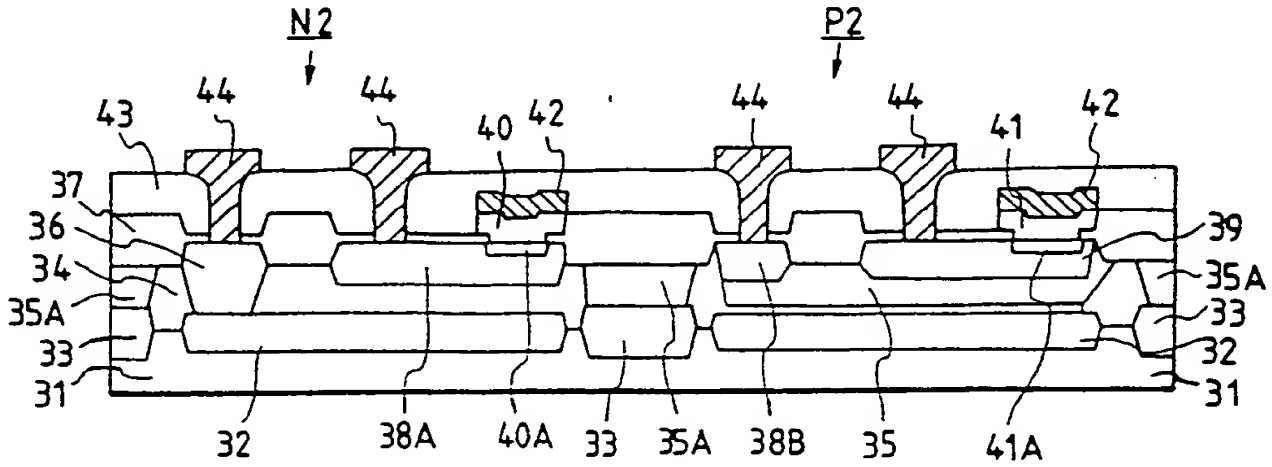


FIG. 18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P2
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44
44
40
42
44
44
41
42
37
36
34
35A
33
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35A
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31
32
38A
40A
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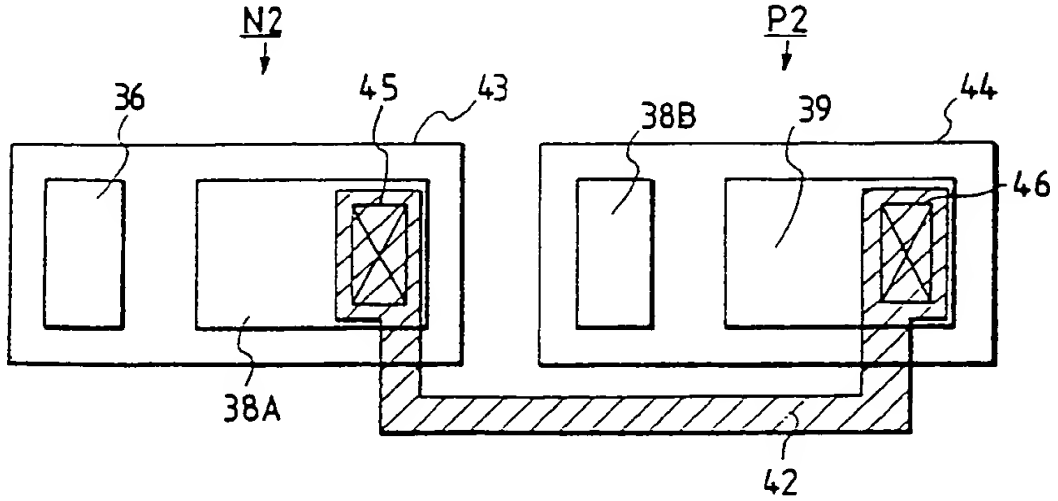
35A
38B
35
41A

FIG. 19


N2
P2
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45
43
38B
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44
46
38A
42

FIG. 20

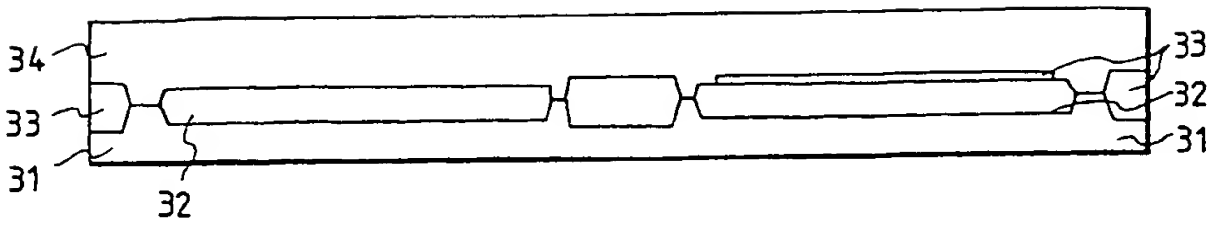


FIG. 21

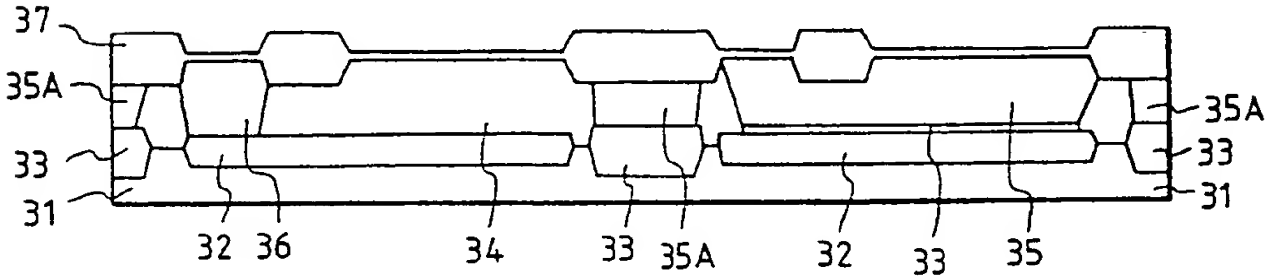


FIG. 22

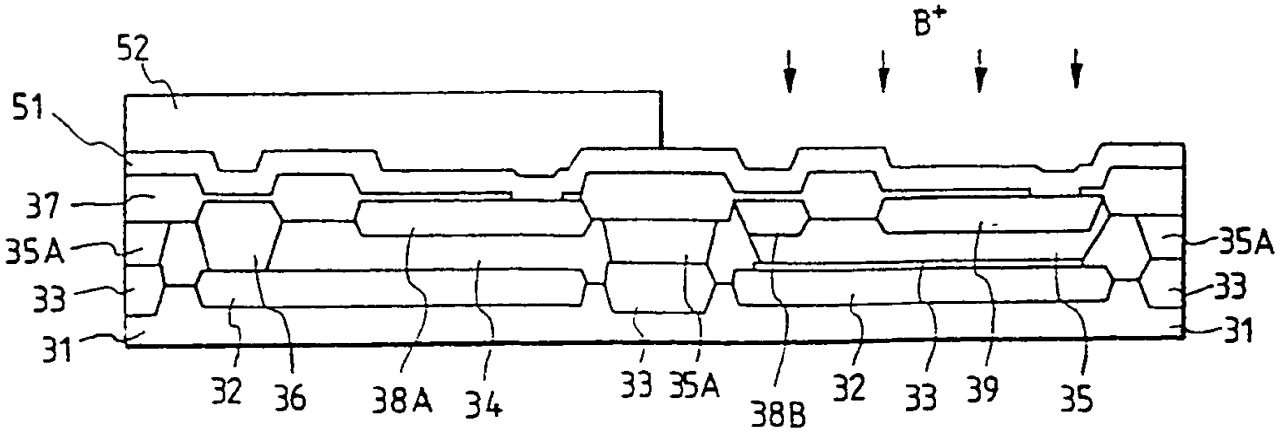


FIG. 23

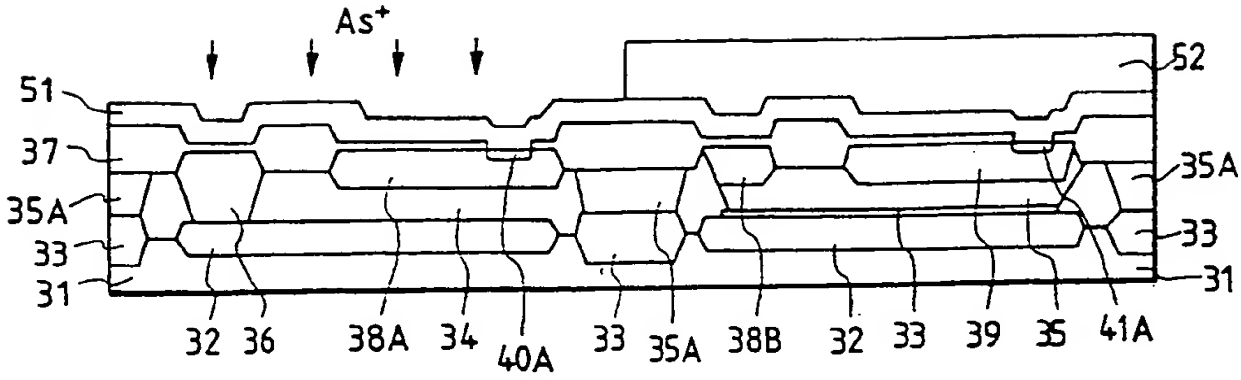


FIG. 24

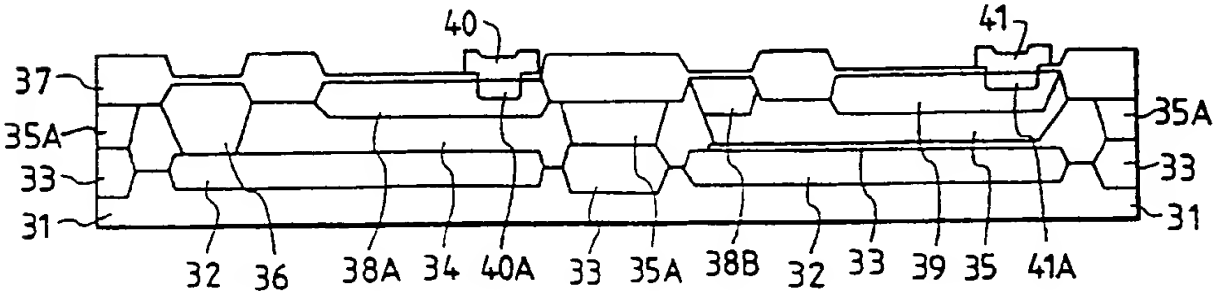


FIG. 25

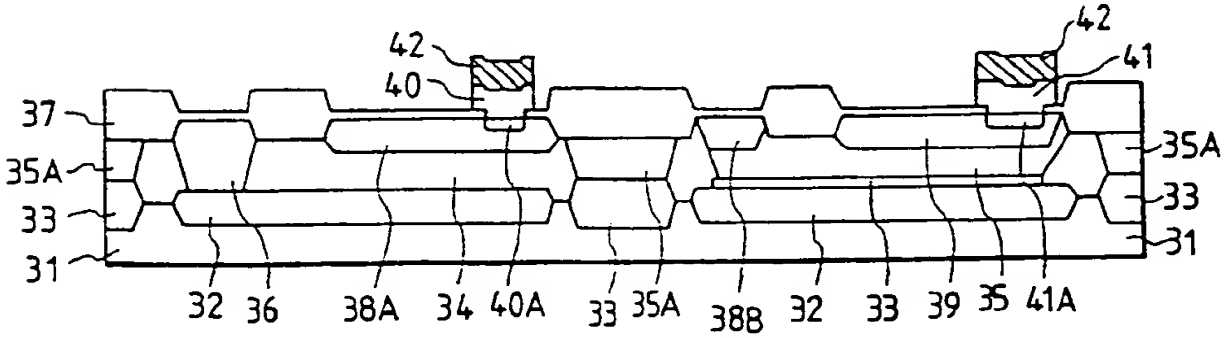


FIG. 26

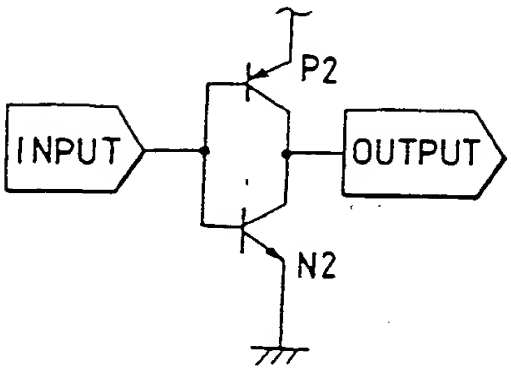
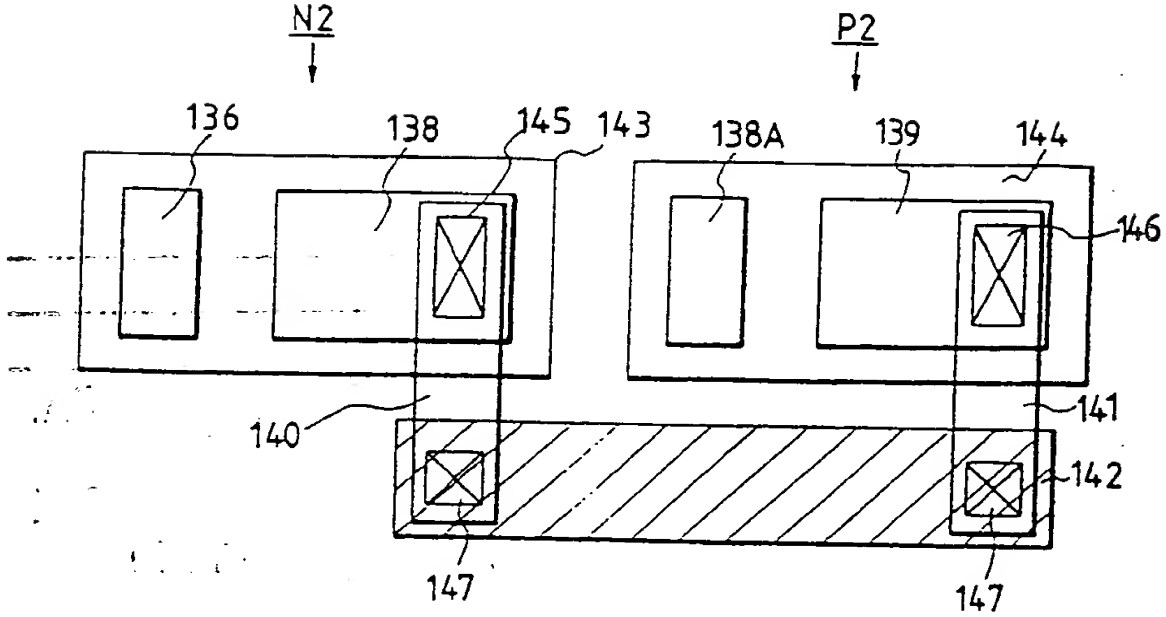

P2
INPUT
OUTPUT
N2

FIG. 27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P2
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145
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138A
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144
146
140
141
142
147
147

DOCKET NO: 8198P2049

SERIAL NO: _____

APPLICANT: Thomas Hancock et al.

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